SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TRIAC DRIVE CIRCUIT FOR OPERATION IN QUADRANTS I AND III

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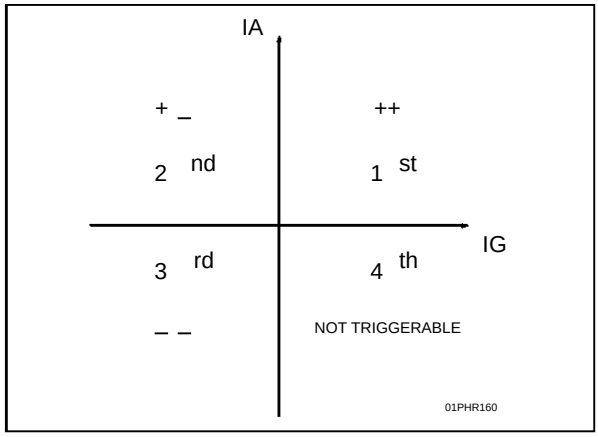
New triacs with high commutation and dv/dt performances are now available on the market.

Generally these triacs are only triggerable in the 3 first quadrants (case of SNUBBERLESS and LOGIC LEVEL triacs) as shown in figure 1.

This paper describes a trigger circuit supplying a negative gate current for quadrants II and III implemented in a system using a positive power supply.

Without a new design, just by adding a capacitor and a diode new W series triacs can replace conventional triac.

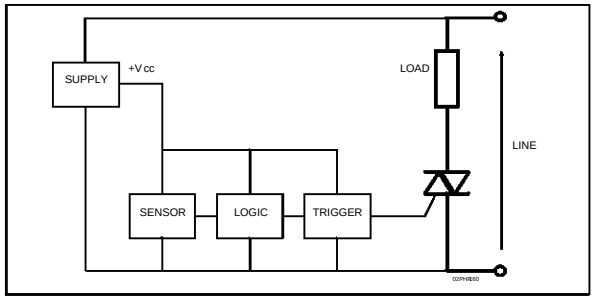
Figure 1 : The quadrants of a W series triac.



I - PRINCIPLE :

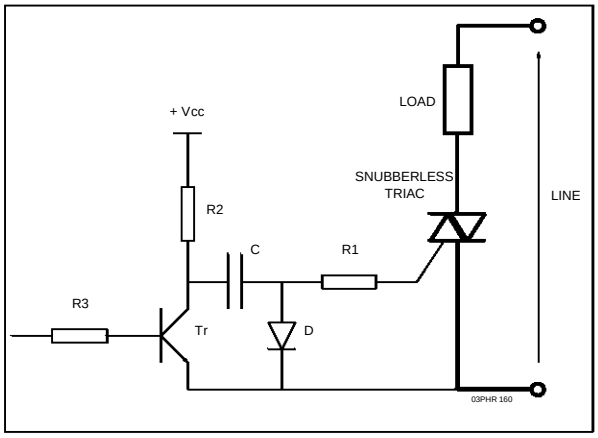
Figure 2 shows the schematic of a system with a sensor, logic and positive power supply (with respect to the anode 1 of the triac).

Figure 2 : Synoptical diagram of a classical system.



To drive the triac in the 2nd and 3rd quadrants a discharge capacitor is used as shown in figure 3.

Figure 3 : Basic diagram of the trigger.



1/ Principle :

- The transistor is switched off, capacitor C is charged through resistance R2 and diode D.

The diode is used to avoid a capacitor load current through the gate of the triac. A schottky diode could be used to improve the voltage drop level lower than the gate non trigger voltage (V_{GD}).

- When the triac is triggered, the transistor Tr is switched on, C is discharged through R1 and Tr and a negative current flows through the gate of the triac.

The capacitor C acts as a differentiation. We have to consider different parameters to define all the components :

- The gate trigger current of the triac (I_{GT})

- The time duration of the gate current

- The latching current (I_L) especially for small or inductive loads.

2/ Review :

Définition of the latching current (I_L) :

The I_L of a triac is the minimum value of the main current which allows the component to remain in the conducting state after the gate current I_G has been removed.

That is to say the gate current has to be higher than I_{GT} until the main current reaches the latcing current.

Example : for the CW SNUBBERLESS triac :
Q1 - Q3 : $I_L$max = 50 mA
Q2 : $I_L$max = 80 mA
With : gate pulse duration of 20µs at Tj = 25°C

I_L max is specified in the CW series triac data sheet.
Statistically, for BW series triacs we can use the K ratio

$K = I_L max / I_{GT} max$

K = 2,3

Two solutions are possible :

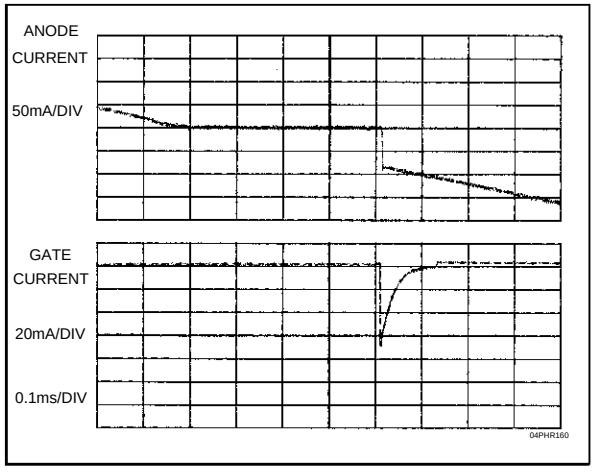
- Triggering with a delay after zero voltage crossing such that the main current is higher than I_L.

- Triggering at zero voltage crossing with a long discharge time in order to have no problem with I_L.

II - THE CASE WITH A RESISTIVE LOAD :

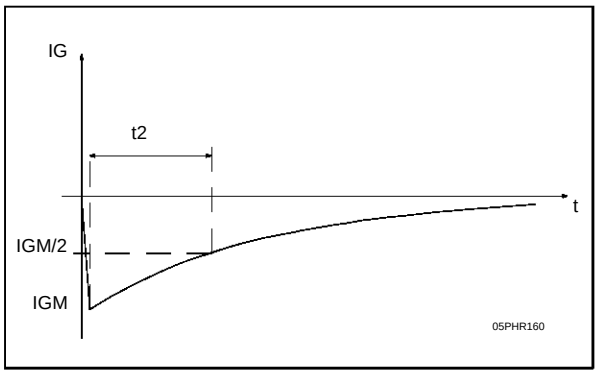
1/ First solution: delayed pulse current (figure 4).

Figure 4 : Triggering with delay t1 after zero crossing.



The gate pulse is shown in Figure 5 :

Figure 5 : Gate pulse.



t1 calculation :

The triac has to be triggered when the main current is higher than the latching current, that is to say t1min is :

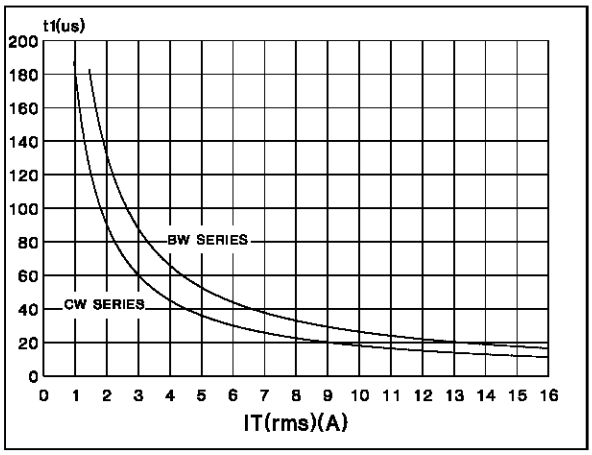
$$t1 = \frac{1}{\omega} arcsin\left(\frac{I_L \max}{I_{RMS}\sqrt{2}}\right)$$

where $\omega = 2 . \pi . f$

I_{RMS} : minimum RMS current in the worst case (depending on line and load dispersion).

The curve given shows the minimum time versus I_{RMS} current through the anode (figure 6).

Figure 6 : t1 time versus I_{RMS} for different latching currents.



The gate current calculation :

I_{GT} is the maximum gate trigger current specified in the data sheet. To ensure a good safety margin and good triggering we have chosen $I_G = 2.I_{GT}$ with a pulse duration t2 higher than 20µs.

All the components can be defined by the following formulae :

R1max = (V_{CC} - V_{GK} - VCE)/(2.I_{GT})

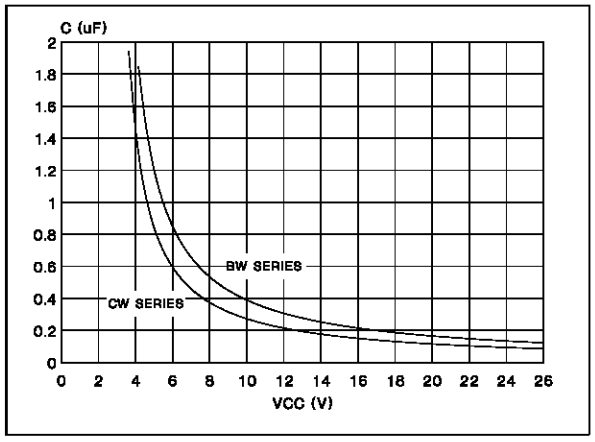
with V_{GK} = 2 V at I_G = 2.I_{GT}

Cmin = t2/(R1.log2) with t2 = 20µs

R2max = 0,001/C

Curve 7 gives the minimum capacitance versus supply voltage for different sensitivity.

Figure 7 : Capacitance value versus supply voltage for different sensitivity.



In this way the RMS current is lower than the full wave current, the RMS current/full wave current ratio is :

$$K^2 = 1 - 2.\frac{t1}{T} + \frac{1}{2\pi}.sin(4\pi\frac{t1}{T})$$

The calculation gives for a 6 Amps CW triac with a 2 Amps sine current and with an IL = 80 mA.

t1 = 90µs

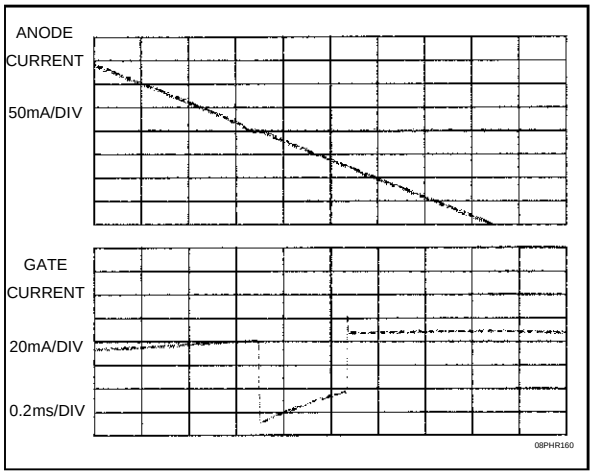
K = 0,99

That means the losses are lower than 1%.

2/ Second solution : Wide current pulse at zero crossing.

It consists of triggering the triac at zero voltage crossing voltage as shown in figure 8.

Figure 8 : Triggering at zero voltage.



Note : In figure 8, the pulse through the transistor base is cancelled before the capacitor is fully discharged to save energy.

All the components can be defined by the following formulae :

$$t2\ \min = \frac{1}{\omega} arcsin\left(\frac{I_L}{I_{RMS}\sqrt{2}}\right) + 20\mu s$$

R1max = (V_{CC}-V_{GK}-V_{CE})/(2.I_GT)

Cmin = t2/(R1.log2)

R2max = 0,001/C

In this way the RMS current is equal to the full wave current.

3/ Comparison between these two solutions :

The calculation of all the components is shown in the following table for 3 differents cases

Figure 9 : Component values for 3 differents cases : triac used : BTA08-600CW (I_{GT} = 35 mA)

	I_{RMS} = 5 A V_{CC} = 10 V		I_{RMS} = 2 A V_{CC} = 5 V		I_{RMS} = 5 A V_{CC} = 5 V	
	with delay	at zero crossing	with delay	at zero crossing	with delay	at zero crossing
t1 min (µs)	36	0	91	0	36	0
t2 min (µs)	20	56	20	111	20	56
R1 max (Ω)	105	105	34	34	34	34
C min (µF)	0.275	0.77	0.85	4.7	0.85	2.37
R2 max (Ω)	3.7	1.3	1.18	0.212	1.18	0.42

III - CASE OF INDUCTIVE LOAD :

With an inductive load another problem occurs : the problem of the phase lag between load current and load voltage.

It can be solved by taking into account :

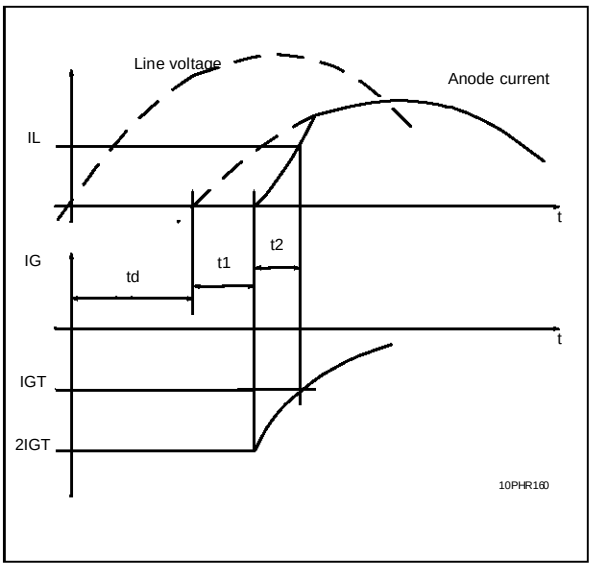
- the maximum phase lag to define a delay time td.

- the latching current to define the time t1

- the inductance to define the time t2= V/L at the moment when the triac is fired (t2 > 20µs) to have an anode current higher than the latching current I_L.

The figure 10 shows the anode current and the gate current in the triac, is the case of an inductive load.

Figure 10 : Current through an inductive load.



If the phase lag is not constant a gate pulse train can be used, the calculation parameters are the same, except for R2 : the capacitor C has to be charged between 2 pulses so the equation is :

R2=(time between 2 pulses)/(5xC)

IV - THE CASE OF A SMALL LOAD :

This trigger circuit can not be effectively used to drive small loads (like valves, fan etc...) because the latching current value is not very small compared to the load current. In this case a DC gate current is needed.

V - CONCLUSION :

In the case of controllers supplied by positive voltage this solution allows of the replacement of conventional triacs used in the 1st and 4th quadrants by SNUBBERLESS or LOGIC LEVEL triacs triggerable only in the 3 first quadrants without a new design but only by adding a capacitor and a diode.

Two configurations are possible :

First solution : Triggering after the zero voltage crossing.
Advantage : capacitor value lower than 1µF.
Disadvantage : the need to have a delay after the zero voltage crossing (delay system needed).

Second solution : Triggering at zero voltage crossing.
Advantage : 100% of the power used in the load.
Disadvantage : capacitor value of a few microfarads.

With inductive loads (motor, transformer, etc...) a pulse train can be used because of the phase lag between current and voltage.

With small loads (valve, fan,...) a DC gate current has to be used to drive the triac because of the latching current.

In case of logic or transistor failure, the capacitor C operates as an open circuit for DC current and avoids all triggering. This factor acts as a safety feature.